IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Before the Board of Patent Appeals and Interferences

In re the Application

Inventor	:	KLOSTERS
Application No.	:	10/531,399
Filed	:	04/14/2005
For	:	DATA PROCESSING APPARATUS THAT PROCESSES INCOMING BITS

APPEAL BRIEF

On Appeal from Group Art Unit 2183

Date: 5/11/2008

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Michael Ure
(Name)

(Signature and Date)

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I. REAL PARTY IN INTEREST

The real party in interest is NXP B.V., the successor in interest to the present assignee of record of the present application, Koninklijke Philips Electronics N.V., and not the party named in the above caption.

II. RELATED APPEALS AND INTERFERENCES

With regard to identifying by number and filing date all other appeals or interferences known to Appellant which will directly effect or be directly affected by or have a bearing on the Board's decision in this appeal, Appellant is not aware of any such appeals or interferences.

III. STATUS OF CLAIMS

Claims 1-9 are pending, all of which stand finally rejected and form the subject matter of the present appeal.

IV. STATUS OF AMENDMENTS

All amendments have been entered. No amendment after final rejection has been submitted.

V. SUMMARY of the CLAIMED SUBJECT MATTER

The present invention relates to a processor that performs programmable bit processing for serial communications. Compared to the prior art, the processor is low in complexity and power consumption. In one embodiment, an input port receives a

communication signal that contains temporally successive bits, and an output port outputs a data word formed from respective ones of the temporally successive bits. A programmable processor circuit coupled to the input port executes a plurality of series of programmed instructions in support of receiving or outputting, each at a time of reception of a respective one of the temporally successive bits, the processor circuit suspending operation each time after executing a respective one of the series of instructions. A synchronization circuit coupled to the processor circuit to triggers execution of respective ones of the series of instructions, each time at the time of reception of the respective one of the temporally successive bits, and, except for a last one of the series of instructions, prior to reception of one or more later bits that contribute to the data word.

The following analysis of independent claim 1 is presented for convenience:

Element	Figure(s)	Paragraph(s) and/or page(s)
1. A data processing apparatus, the apparatus comprising:		
an input port for receiving a communication signal that contains temporally successive bits;	Fig. 1, 14; Fig. 2	Page 3, lines 22-33
an output port for outputting a data word formed from respective ones of the temporally successive bits;	Fig. 1, output of block 100; Fig. 6, output of block 46	Page 10, lines 29-31
a programmable processor circuit coupled to the input port, the processor executing a plurality of series of programmed instructions in support of said receiving or said outputting, each at a time of reception of a respective one of the temporally successive bits, the	Fig. 1, 100; Fig. 6	Page 3, lines 22-33; page 4, line 1 to page 5, line 5.

processor circuit suspending operation each time after executing a respective one of the series of instructions;		
a synchronization circuit coupled to the processor circuit to trigger execution of respective ones of the series of instructions, each time at the time of reception of the respective one of the temporally successive bits, and, except for a last one of the series of instructions, prior to reception of one or more later bits that contribute to the data word.	Fig. 1: 104, 106, 108; Fig. 2	Page 5, lines 6-27

The following analysis of independent claim 9 is presented for convenience:

Element	Figure(s)	Paragraph(s) and/or page(s)
9. A method of processing data, the method comprising:		
receiving a communication signal that contains temporally successive bits; outputting a data word derived from a plurality of the successive bits;	Fig. 1, 14; Fig. 2	Page 3, lines 22-33
executing a plurality of series of programmed instructions in support of receiving and/or outputting, each at a time of reception of a respective one of the temporally successive bits, suspending execution of the series of instructions each time after executing a respective one of the series of instructions;	Fig. 1, 100; Fig. 6	Page 3, lines 22-33; page 4, line 1 to page 5, line 5.
triggering execution of respective ones of the series of instructions, each time at the time of reception of the respective one of the temporally successive bits, and, except for a last one of the series of instructions, prior to reception of one or more later bits that contribute to the data word.	Fig. 1: 104, 106, 108; Fig. 2	Page 5, lines 6-27

VI. GROUNDS of REJECTION to be REVIEWED ON APPEAL

The issues in the present matter are whether:

1. under 35 USC 102, claims 1, 2 and 4-9 are anticipated by Hao.

2. under 35 USC 103, claim 3 is unpatentable over Hao in view of Wishnuesky.

VII. ARGUMENT

I. Rejection of Claims 1, 2 and 4-9 as Anticipated by Hao

At the most basic level, a principal difference between Hao and the present invention is that the processor of the present invention is programmable, whereas the apparatus of Hao is dedicated, or hardwired. The use of dedicated or hardwired bit processors is described in the BACKGROUND portion of the present specification.

More particularly, in Hao, bit-level operations are performed by the hardwired autobaud state machine 20. Such hardwired bit-level processing is described in Hao as being necessary to keep up with ever-increasing bit rates. The autobaud state machine does not execute a series of programmed instructions. Nor does the autobaud module 12 considered as a whole "execute a plurality of series of programmed instructions in support of receiving or outputting, each at a time of reception of a respective one of the temporally successive bits, the processor circuit suspending operation each time after executing a respective one of the series of instructions" as claimed. The autobaud state machine, in particular, is incapable of suspending operation. A state machine "waiting" for the start bit of a next character is certainly not the same as suspending operation.

Finally, in Hao, there is no "synchronization circuit coupled to the processor circuit to trigger execution of respective ones of the series of instructions [i.e., *programmable* instructions], each time at the time of reception of the respective one of the temporally successive bits." The function of the baud rate determination means 32 of Hao, on the other hand, is simply to determine a value of M and communicate that value to the autobaud state machine 20 and the baud rate generator 30. As seen in Table 2, M is a divisor value that relates the baud rate to the system clock. The communication of M to the autobaud state machine and the baud rate generator, while it may influence hardwired operation of the circuit, does not trigger the execution of a series of *programmable* instructions as claimed.

In fact, there are no *instructions* in Hao, programmable or otherwise. A sequence of instructions are stored in advance and a particular instruction is selected for execution at a particular time. Note, for example, the structure of the processor 100 of Fig. 6 of the present specification. A program counter 48 applies an address to an instruction memory 102, which applies a selected instruction to a logic unit 42. Such a construction is characteristic of a processor that executes instructions. There is no corresponding structure in Hao. Rather, in Hao, as in any typical state machine, there are state registers 24, the contents of which are changed to register state changes during the course of operation of the state machine. There are no instructions stored in advance.

Accordingly, Hao is not believed to anticipate claim 1.

With regard to dependent claims 2 and 4-8, these claims depend from independent claim 1, which has been shown to be patently distinguishable over the cited reference. Accordingly, these claims are also patently distinguishable and allowable over the cited references by virtue of their dependency upon an allowable base claim.

I. Rejection of Claim 3 as Unpatentable Over Hao in View of Wishnuesky

Wishnuesky does nothing to remedy the deficiencies of Hao as described above. Accordingly, claim 3 is believed to patentably define over the cited references.

In view of the above, applicant submits that all of the above referred-to claims are patentable over the teachings of the cited references.

VIII. CONCLUSION

In view of the above analysis, it is respectfully submitted that the referenced teachings, whether taken individually or in combination, fail to anticipate or render obvious the subject matter of any of the present claims. Therefore, reversal of all outstanding grounds of rejection is respectfully solicited.

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IX. APPENDIX: THE CLAIMS ON APPEAL

1. A data processing apparatus, the apparatus comprising:

an input port for receiving a communication signal that contains temporally successive bits;

an output port for outputting a data word formed from respective ones of the temporally successive bits;

a programmable processor circuit coupled to the input port, the processor executing a plurality of series of programmed instructions in support of said receiving or said outputting, each at a time of reception of a respective one of the temporally successive bits, the processor circuit suspending operation each time after executing a respective one of the series of instructions;

a synchronization circuit coupled to the processor circuit to trigger execution of respective ones of the series of instructions, each time at the time of reception of the respective one of the temporally successive bits, and, except for a last one of the series of instructions, prior to reception of one or more later bits that contribute to the data word.

2. A data processing apparatus according to claim 1, wherein the programmable processor is programmed to compute cumulative information, corresponding to a function of a combination of the bits from which the data word is formed, each series of instructions being programmed to add a contribution to the cumulative information of the respective one of the temporally successive bits at the time of reception of which the series is executed.

3. A data processing apparatus according to claim 2, wherein said cumulative information comprises one or more parity bits.

4. A data processing circuit according to claim 1, wherein the processor circuit is constructed sequence instruction execution using handshake signals, execution of each of the instructions of the series being triggered by a respective request signal, execution of each instruction of the series, except for a last instruction in each series, generating the request signal for a next one of the instructions in the series, the synchronization circuit being coupled to apply the request signals for the initial one of the instructions in the series.

5. A data processing apparatus according to claim 1, wherein the synchronization circuit contains an adaptable timer circuit, arranged to adapt a frequency of triggering the execution of the series of instructions under control of a timing of transitions in the communication signal.

6. A data processing apparatus according to claim 5, wherein the adaptable timer circuit is arranged to measure a duration of a synchronization interval in the communication signal preceding bits that contribute to the data word, and to set the frequency that will be used to trigger execution of the series of instructions dependent on the measured duration.

7. A data processing apparatus according to claim 6, wherein the timer circuit is arranged

to detect presence or absence of a validation part in the communication signal prior to bits that contribute to the data word, the timer circuit generating execution trigger signals only upon detection of the presence of the validation part.

8. A data processing apparatus according to claim 1, wherein the processor circuit is designed to execute only instructions with one bit operand data.

9. A method of processing data, the method comprising:

receiving a communication signal that contains temporally successive bits;

outputting a data word derived from a plurality of the successive bits;

executing a plurality of series of programmed instructions in support of receiving and/or outputting, each at a time of reception of a respective one of the temporally successive bits, suspending execution of the series of instructions each time after executing a respective one of the series of instructions;

triggering execution of respective ones of the series of instructions, each time at the time of reception of the respective one of the temporally successive bits, and, except for a last one of the series of instructions, prior to reception of one or more later bits that contribute to the data word.

X. APPENDIX: RELATED PROCEEDINGS

NONE

XI. APPENDIX: EVIDENCE

NONE